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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,898	12/14/2001	Hsing-Ya Tsao	AP01-008	9617

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EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary		
	Examiner	**Art Unit**
	Connie c. Yoha	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*
4) ☐ Interview Summary (PTO-413) Paper No(s).
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 3/7/02 was considere3.

2. Claims 1-39 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Ratnakumar, Pat. No. 6114724.

With regard to claim 1 and 18, Ratnakumar discloses a two transistor flash memory cell, having: a floating gate storage device (fig. 3A, 326) with a shallow N+ source region (fig. 3A, 306), an access device (fig. 3A, 328) with a shallow N+ drain region (fig. 3A, 306), said storage device (fig. 3A, 326) and said access device (fig. 3A, 328) share a shallow N+ common region (fig. 3A, 306) for the storage device and a source for the access device (col. 4, line 18-20) (also with regard to claim 19, 20, and 24), said source, drain and common regions producing a symmetrical memory cell in which size of the memory cell is limited by characteristics of a read operation (col. 4,

With regard to claim 2, Ratnakumar discloses wherein the storage device and the access device are NMOS devices (fig. 3A).

With regard to claim 3, Ratnakumar discloses wherein the floating gate storage device is coupled in series with the access device to form a cell to create a compact flash array for programmable logic devices (fig. 13).

With regard to claim 4, Ratnakumar discloses wherein a channel erase operation using Fowler-Nordheim (FN) tunneling is used to erase said floating gate storage device (col. 7, line 47-48) and a channel program operation using FN tunneling is used to program said floating gate storage device (col. 8, line 5-7) (also with regard to claim 14-16, 21 and 32).

With regard to claim 5, Ratnakumar discloses wherein the channel erase operation decreases a threshold voltage of the floating gate storage device (col. 7, line 50-56) and the channel program operation increases the threshold voltage of the floating gate storage device (col. 8, line 26-32)

With regard to claim 6, Ratnakumar discloses wherein a low voltage gradient is produced from source to drain of the storage device during the channel program operation which allows a shorter length for high density applications (col. 9, line 66-col. 10, line 17).

With regard to claim 7, Ratnakumar discloses wherein said source region (fig. 3A, 304), said drain region (fig. 3A, 308) and said common region (fig. 3A, 306) are located in a P-well within a deep N-well on a P-substrate (fig. 3B) (also with regard to

With regard to claim 9, Ratnakumar discloses wherein a tunnel oxide of the storage device and a gate oxide of the access device are created within a same process step (col. 4, line 58-60) (also with regard to claim 10, and 22).

With regard to claim 11 and 23, Ratnakumar discloses a flash memory array for use in high density and low voltage applications comprising: an array of two transistor flash memory cells (fig. 13) comprising a storage transistor (fig. 13, 1320) and an access transistor (fig. 13, 1318) arranged in rows and columns and formed with cells containing a floating gate storage device (fig. 13, 1320) and an access device (fig. 13, 1318), said cells in a column are coupled by bit lines (fig. 13, 1316) and source lines (fig. 13, 1322) (also with regard to claim 13, 26 and 27) , said bit lines are decoded by an inherent bit line decoder (also with regard to claim 28) and the source lines are decoded by an inherent source decoder (also with regard to claim 29), the cells in a row are coupled by word lines (fig. 13, 1326) and access lines (fig. 13, 1317), the word lines (fig. 13, 1326) coupled to control gates of the storage devices (fig. 13, 1320) and are controlled by a word line decoder (fig. 13, 1304) (also with regard to claim 31), the access lines (fig. 13, 1317) are coupled to gates of the access devices (fig. 13, 1318) and are controlled by an access decoder (fig. 13, 1310) (also with regard to claim 30).

With regard to claim 12, Ratnakumar discloses wherein the two transistor memory cells are arranged such that channels of the storage transistor and the access transistor are oriented vertically (fig. 3A, fig. 3B, fig. 13).

With regard to claim 17, Ratnakumar discloses wherein memory cells that are not selected for a memory operation are biased to eliminate disturb conditions (col. 11, line 20-31).

Drafted as Method claim

4. As per claim 33-39 encompass the same scope of invention as to that of claim 1-32 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Bergemont et al (6177315) and Hong et al (6396745) disclose a memory device.

6. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The examiner can normally be reached on Mon - Fri from 8:00 A.M. to 5:30 P.M. The

phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

June 2003

Connie C. Yoha

Patent Examiner

Art Unit 2818